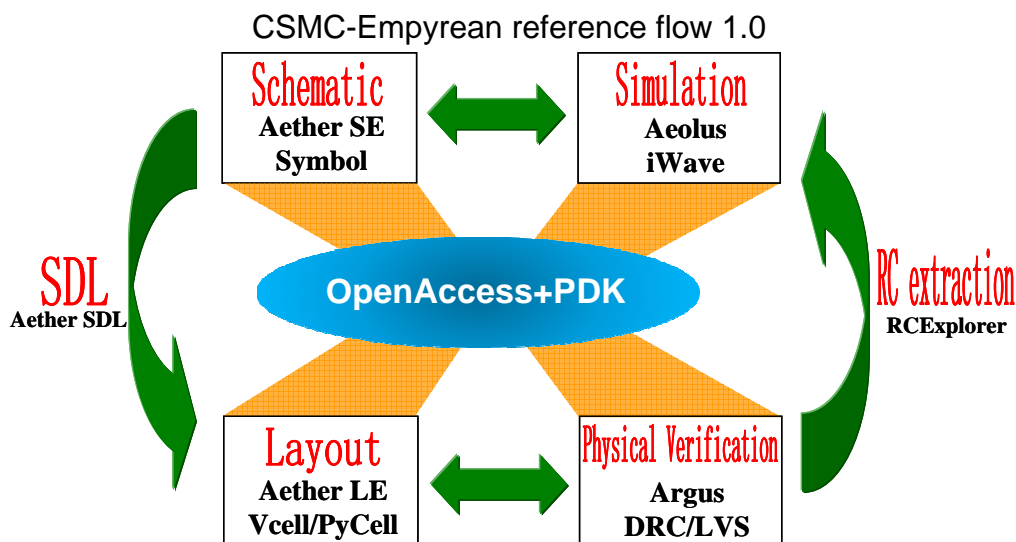


CSMC-Empyrean reference IC design flow 1.0

- ◆ Empyrean is the China largest EDA vendor and has independent intellectual property rights. Empyrean supply the total solution for Custom/Analog IC design. Empyrean and CSMC joint to develop PDK base on CSMC process. It allows designers to give full play the powerful EDA tools and enable designers in the shortest time to complete high-quality IC design.
- ◆ This reference flow includes schematic capture, SPICE simulation, layout design, physical verification, parasitic RC extraction and post-simulation.



Reference Flow Step and Feature

- ◆ Schematic Capture by Aether Schematic Editor
 - EDIF in
 - Hierarchy schematic edit
- ◆ SPICE Simulation by Aeolus / Waveform Viewer by iWave
 - 100% SPICE precision
 - Compatible standard tools model, netlist and analysis syntax
 - Support MT(multi-thread)
- ◆ Layout Design by Aether Layout Editor
 - OpenAccess
 - Vcell/PyCell
 - Hierarchy SDL
- ◆ DRC/LVS by Argus
 - Compatible standard tools syntax
 - Support GUI and integrated in Aether
 - High performance LVL(Layout vs Layout)
- ◆ RC Extraction by RCExplorer
 - 3D field solver for high accuracy extraction
 - Support un-routed and partial route net extraction with built-in routing engine
 - Support P2P(Point to Point) resistance extraction and analysis
- ◆ Post Simulation by Aeolus / Waveform Viewer by iWave

Detail refer to [Http://www.empyrean.com.cn](http://www.empyrean.com.cn)