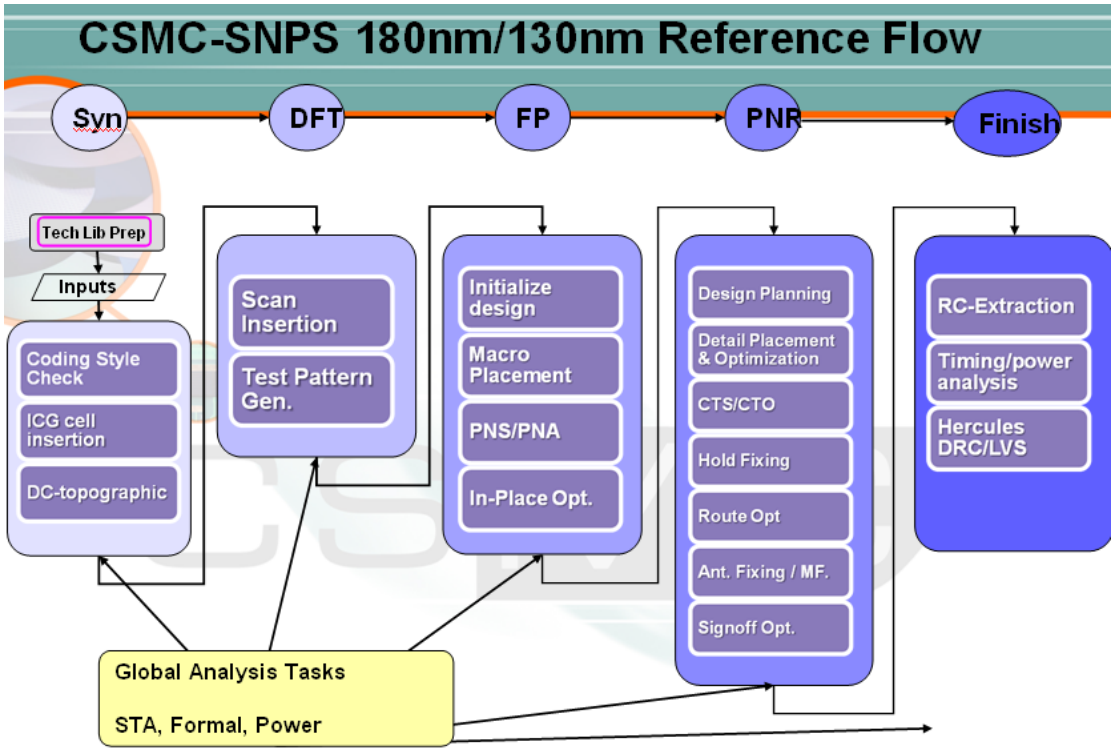
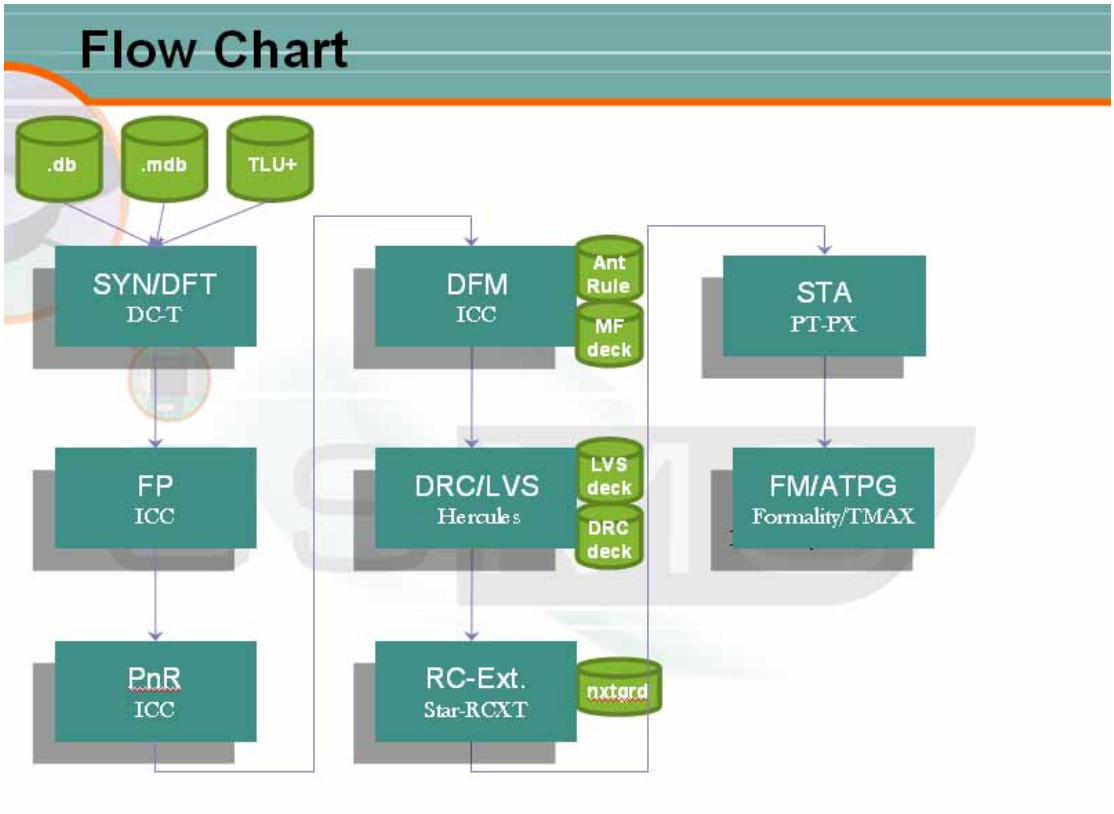
CSMC-SNPS 180/130nm Reference Flow

- CSMC-Synopsys 180nm/130nm reference design flow is a fully validated hierarchical design flow to address multimillion gate designs with high timing complexity requirements. This flow allows designer shorten their design time by eliminating painful iterations. Based on consistent timing engine, designers can have confidence in achieving good quality of results.
- The reference design flow demonstrates a complete solution from RTL to verified GDSII using Synopsys tools, CSMC 180nm/130nm process. It provides concepts of the design flow steps such that it can be implemented or adapted to any customer design environment.





Flow Step and Feature

- Synthesis by DC
  - DC Topographical technology
  - Clock gating by Power Compiler
- Design-for-test by DFT Compiler
- Place and Route by ICC
  - Design Planning (Flat/Hierarchical, PNA/PNS)
  - Detail Placement & Optimization
  - Clock Tree & Optimization
  - Detail Routing & Optimization
- Basic DFM by ICC
  - Antenna Repair
  - Dummy Metal Filling
- RC Extraction by Star-RCXT
- Common Analysis
  - STA and Power by PT-PX
  - Formal
- Hercules signoff
  - Hercules DRC
  - Hercules LVS
- TetraMAX ATPG
  - Patter generation